UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,337	06/25/2001	In Duk Song	8733.425.00	5925

30827 7590 07/02/2003

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER
CHOWDHURY, TARIFUR RASHID

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,337	SONG, IN DUK	
	Examiner	Art Unit	
	Tarifur R Chowdhury	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *21 April 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

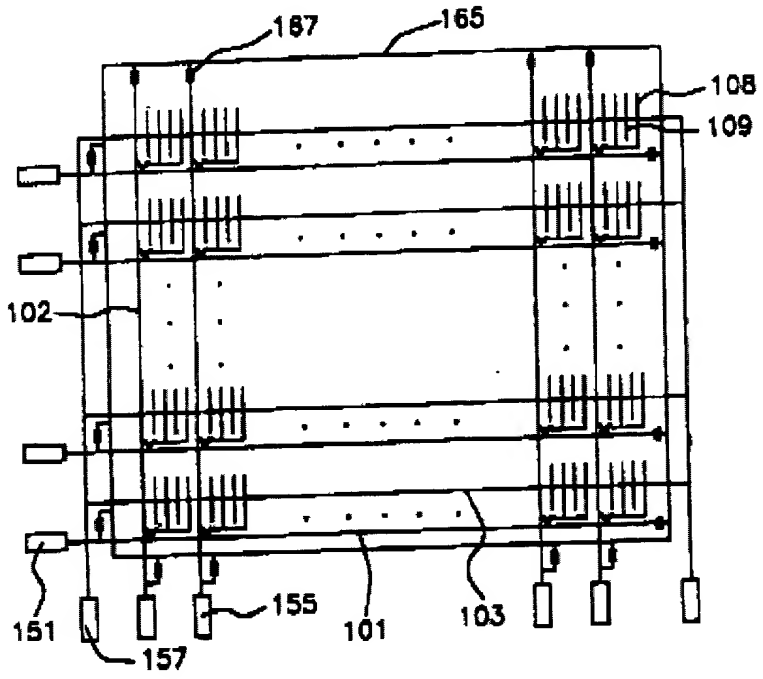
> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. **Claims 1, 2 and 6-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Komatsu, USPAT 6,335,770.**

3. Komatsu discloses in col. 5, lines 40-65 and shows in Fig. 5 (reproduced below), an in-plane switching type liquid crystal display device comprising:

- a plurality of data lines (102) for applying data signals to a thin film transistor array;
- a plurality of gate lines (101) for applying gate signals to the thin film transistor array;
- a plurality of gate links extended from the plurality of gate lines (101) into an outer area of the thin film transistor array; and
- a plurality of common voltage lines connected to common voltage pads (157), being provided in such a manner to cross the plurality of gate links, for applying a common voltage to the thin film transistor array.

FIG.5



Komatsu also shows in Fig. 5 that the common voltage lines are parallel to the gate lines (101).

Accordingly, claims 1, 2 and 6 are anticipated.

As to claim 7, Komatsu shows in Fig. 5 that the in-plane switching liquid crystal display device further comprising:

- a plurality of gate pads (151) connected to the gate links and electrically disposed between the gate links and an external power source; and
- a plurality of common voltage pads (157) connected to the common voltage lines and electrically disposed between the common voltage lines and the external power source.

Accordingly, claim 7 is anticipated.

As to claims 8-11 and 14, Fig. 5 of Komatsu also shows that the gate pads (151), data pads (155) and the common voltage pads (157) are located in an area outside of the thin film transistor array.

As to claims 12 and 13, Komatsu also shows in Fig. 5 that at least one common line that is parallel to the data line (102) crosses the gate lines (101) in an area between the gate pads (151) and the thin film transistor array.

As to claims 15 and 16, Komatsu shows in Fig. 5 that at least one common line crosses the data lines (102) in an area between the data pads (155) and the thin film transistor array.

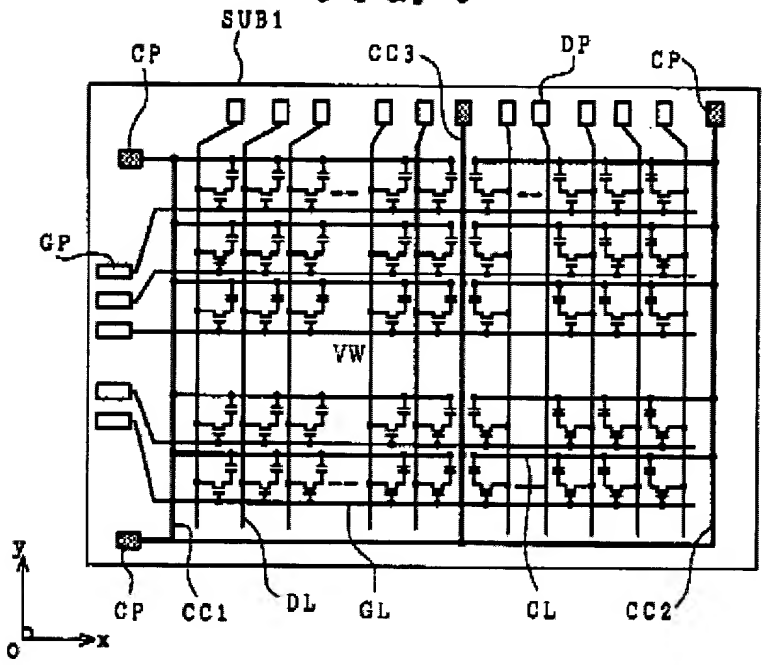
4. Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Ashizawa et al., (Ashizawa), USPAT 6,456,350.

5. Ashizawa discloses in col. 9, lines 27-67 and shows in Fig. 6, an in-plane switching type liquid crystal display device comprising:

- a plurality of data lines (DL) for applying data signals to a thin film transistor array;
- a plurality of gate lines (GL) for applying gate signals to the thin film transistor array;
- a plurality of gate links extended from the plurality of gate lines (GL) into an outer area of the thin film transistor array; and

- a plurality of common voltage lines (CC1, CC2) connected to common voltage pads (CP), being provided in such a manner to cross the plurality of gate links, for applying a common voltage to the thin film transistor array.

FIG. 6



Ashizawa also shows (Fig. 6) that plurality of gate pads (GP) that are located outside of the thin film transistor array are connected to the gate links and electrically disposed between the gate links and an external power source.

Ashizawa also shows (Fig. 6) that a plurality of data pads (DP) are connected to the data links.

Ashizawa further shows (Fig. 6) that a common voltage line is parallel to the data lines (DL) and a common voltage line is parallel to the gate line (GL).

Accordingly, claims 1, 2 and 6-16 are anticipated.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashizawa as applied to claims 1, 2 and 6-16 above.

8. As to claims 3-5, standard driving common voltage for driving an LCD is approximately 5Vand standard gate low voltage ranges from 0V to –5 V whereas standard gate high voltage is approximately 20V. Therefore, it would have obvious to apply standard voltages to the common voltage line or the gate signal line to avail a proven driving method of a liquid crystal display.

Response to Arguments

9. Applicant's arguments see page 7, second paragraph, filed on 04/21/03, with respect to the double patenting rejection have been fully considered and are persuasive. The double patenting rejection of claims 1-16 has been withdrawn.

10. Applicant's arguments filed on 04/21/03 have been fully considered but they are not persuasive.

In response to applicant's argument that Ashizawa and Komatsu do not disclose the limitation such as, "a plurality of common voltage lines, being provided in such a manner to cross the plurality of gate links, for applying a common voltage to the thin film transistor array.", it is respectfully pointed out to applicant that Ashizawa discloses in

col. 9, lines 27-67 and shows in Fig. 6 and Komatsu discloses in col. 5, lines 40-65 and shows in Fig. 5, that the a plurality of common voltage lines connected to common voltage pads (157), being provided in such a manner to cross the plurality of gate links, for applying a common voltage to the thin film transistor array.

Thus the rejection was proper and thus maintained.

In response to applicant's argument that Ashizawa and Komatsu do not disclose the limitation such as, "a plurality of common voltage lines parallel to the gate lines and crossing the gate links.", it is respectfully pointed out to applicant that Ashizawa and Komatsu shows in Figs. 6 and 5 respectively that a part of the plurality of common voltage lines are indeed parallel to the gate lines and crossing the gate links.

Therefore, the rejection was proper and thus maintained.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tarifur R Chowdhury whose telephone number is (703) 308-4115. The examiner can normally be reached on M-Th (6:30-5:00) Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (703) 305-3492. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7005 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

T. Chowdhury
Primary Examiner
Technology Center 2800

TRC
June 27, 2003